DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Course	ECE 35800 - Introduction to VHDL
Type of Course	Required for CmpE Program, Elective for EE Program
Catalog Description	Introduction to the design of digital systems using VHDL hardware description language. Emphasis on how to write VHDL that will map readily to hardware. Projects assigned using commercial-grade computer-aided design (CAD) tools for VHDL-based design, VHDL simulation, and synthesis.
Credits	3
Contact hours	3
Prerequisite Courses	ECE 27000, ECE 22900
Corequisite Courses	None
Prerequisites by Topics	Familiarity with the fundamentals of digital logic design – including combinational logic design, logic minimization, and state machine design; prior programming experience in a structured programming language highly desirable as preparation for learning to write VHDL code
Textbook	*Circuit Design and Simulation with VHDL*, by Volnei A. Pedroni, The MIT Press, current edition.
Course Objectives	At the end of this course, students should be able to: • Code in VHDL for synthesis • Decompose a digital system into a controller (FSM) and datapath, and code accordingly • Write VHDL testbenches • Synthesize and implement digital systems on FPGAs • Understand behavioral, non-synthesizable VHDL and its role in modern design
Course Outcomes	Students who successfully complete this course will have demonstrated the ability to:

1. Be able to describe combinational and sequential components using VHDL. (2)
2. Be able to draw schematic from VHDL description (1)
3. Be able to simulate VHDL modules and analyze/interpret simulated data and waveform. (6)
4. Be able to analyze with ASM-chart controller and datapath (2)
5. Be able to design complex digital system, describe it in VHDL.   (1)
6. Be able to use modern electronic design tools for synthesis, and simulation (7)

Lecture Topics

1. Course overview, VHDL synthesis and simulation design flow
2. Combinational logic design - schematic and VHDL
3. Use of test benches, timing constraints, optimization trade-offs
4. Sequential logic functions in VHDL
5. State machine design in VHDL
6. System level design in VHDL
7. Synthesis on FPGAs
8. Advanced VHDL topics

Computer Usage   High

Laboratory Experience   High

Design Experience   High

Coordinator   Guoping Wang, Ph.D.

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